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AMENDMENTS TO THE SPECIFICATION

Please delete the section entitled "SUMMARY OF THE INVENTION" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

[0020.1] The present invention, among other applications, is directed to solving these and other problems and disadvantages of the prior art. The present invention provides a superior technique for performing cryptographic operations within a microprocessor. In one embodiment, an apparatus for performing cryptographic operations is provided. The apparatus includes a ~~cryptographic instruction~~fetch logic and execution logic. The fetch logic is disposed within a microprocessor, and is configured to receive a cryptographic instruction ~~is received by a microprocessor~~ as part of an instruction flow executing on the microprocessor. The cryptographic instruction prescribes one of the cryptographic operations, and also prescribes that an intermediate result be generated. The execution logic is disposed within the microprocessor and is operatively coupled to the cryptographic instruction. The execution logic executes the one of the cryptographic operations, and generates the intermediate result.

[0021] One aspect of the present invention contemplates an apparatus for performing cryptographic operations. The apparatus has a control word and a cryptography unit. The control word prescribes that an intermediate result be generated during execution of one of the cryptographic operations. The cryptography unit is within a microprocessor and is configured to execute the one of the cryptographic operations responsive to receipt of a cryptographic instruction within an instruction flow that prescribes the one of the cryptographic operations, where the cryptographic instruction is fetched from memory by fetch logic in the microprocessor, and where the cryptographic instruction also references the control word.

[0022] Another aspect of the present invention provides a method for performing cryptographic operations. The method includes, within a microprocessor, fetching a cryptographic instruction from memory prescribing~~via a cryptographic instruction, prescribing~~ that an intermediate result be generated during execution of one of a plurality

of cryptographic operations; and, ~~within~~ awithin the microprocessor, receiving the cryptographic instruction, and generating the intermediate result when executing the one of the cryptographic operations.